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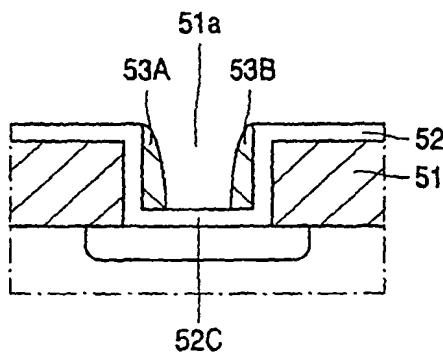
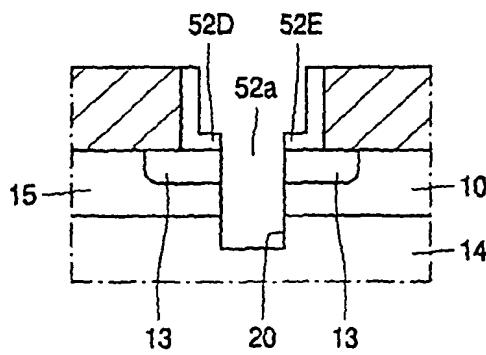
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MANUFACTURING A TRENCH-GATE SEMICONDUCTOR DEVICE AND CORRESPONDING DEVICE



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(57) Abstract: The manufacture of a trench-gate semiconductor device, for example a power transistor or a memory device includes the steps of forming at a surface (10a) of a semiconductor body (10) a first mask (51) having a first window (51a), providing a thin layer of a second material (52) in the first window (51a), forming an intermediate mask (53A, 53B) of a third material having curved sidewalls and using the intermediate mask (53A, 53B) to form two L-shaped parts (52A, 52D and 52B, 52E) of the second material with a second window (52a) which is used to etch a trench-gate trench (20). The rectangular base portion (52D, 52E) of each L-shaped part ensures that the trench (20) is maintained narrow during etching. Narrow trenches are advantageous for low specific on-resistance and low RC delay in low voltage cellular trench-gate power transistors. Narrow deep trenches are also advantageous for cell density in DRAM devices where a memory cell has a switching transistor cell surrounded by a trench-gate and a storage capacitor in a lower part of the same trench.

INTERNATIONAL SEARCH REPORT

International Application No

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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7	H01L21/336	H01L21/331	H01L21/8242	H01L21/338	H01L21/308
	H01L29/78	H01L29/739	H01L27/108	H01L29/812	

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

WPI Data, PAJ, INSPEC, COMPENDEX, IBM-TDB, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	NAM K S ET AL: "A novel simplified process for fabricating a very high density p-channel trench gate power MOSFET" IEEE ELECTRON DEVICE LETTERS, vol. 21, no. 7, July 2000 (2000-07), pages 365-367, XP000951986 IEEE, NEW YORK, NY, USA ISSN: 0741-3106 paragraphs II, III; figure 1	16-19
A	---	1-4, 6
X	WO 99 54918 A (KONINKLIJKE PHILIPS ELECTRONICS NV ET AL) 28 October 1999 (1999-10-28) cited in the application page 7, line 14 -page 10, line 31; figures 1-9	16-19
A	---	1-4, 6, 7
	-/-	

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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- *&* document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl. Fax: (+31-70) 340-3016	Authorized officer Morvan, D

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 177 576 A (KIMURA S ET AL) 5 January 1993 (1993-01-05) column 5, line 27 -column 8, line 37; figures 6A-6V -----	20
A	KAGA T ET AL: "Advanced OSELO isolation with shallow grooves for high-speed submicrometer ULSIs" IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 35, no. 7, July 1988 (1988-07), pages 893-898, XP002198976 IEEE, NEW YORK, NY, USA ISSN: 0018-9383 page 893, lines 1-13 of paragraph II; figure 3 -----	1,2,15
A		1,2,4

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
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				20-01-1992